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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,500	08/11/2000	Robert Gelinas	07030.0011-00	7608

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EXAMINER

TSAI, HENRY

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 09/30/2003

9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/637,500	Applicant(s) GELINAS ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 7/11/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9 and 10 is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities: in claim 8, line 5, before "circuit" -a- should be inserted. Appropriate correction is required.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "High-performance digital signal processor(DSP) comprising two execution pipelines capable of executing RISC instructions"

3. The disclosure is objected to because of the following informalities:

at page 2, line 2, "Dsp" should read -DSP-;

at page 5, line 13, "coprocessor" should read
-Coprocessor-;

at page 5, line 20, "196" should read
-198-, and "198" should read -196-;

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at page 9, line 2, "and" should be deleted;

at page 9, line 10, it is not clear what is meant by "dest of 10";

at page 8, line 15, after "leB", -ld0- should be inserted;

at page 10, line 1, "272" should read -268-, and "274" should read -270-;

at page 12, line 2, "44" should read -440-; and

at page 21, line 13, "cbe 3" should read -cbe 2-.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly

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or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Davis et al. (US 5,459,843).

Davis et al. discloses, as claimed, a digital signal processor comprising: two execution pipelines (See Col. 5, lines 28-33, and Fig. 6, (A) processing pipeline and (B) processing pipeline) capable of executing RISC instructions (See Col. 5, lines 28-29); instruction fetch logic (116, se Fig. 6) that simultaneously fetches two instructions and routes them to respective pipelines (See Col. 5, lines 30-33); and control logic (123, see Fig. 6 and Col. 5, lines 46-49) to allow the pipelines to operate independently.

As to claim 2, Davis et al. also discloses: the instruction fetch logic (123, see Fig. 6 and Col. 5, lines 46-49) includes logic that fetches dual SIMD instructions (note as shown in Col. 8, lines 19-26, n execute units inherently provide the function to process SIMD instructions).

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6. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Gatherer et al. (6,298,366).

Referring to claim 7, Gatherer et al. discloses, as claimed, a digital signal processor (100, see Fig. 1, and Col. 3, lines 11-14) comprising: a register pair (225, and 237, see Fig. 7) ; and means (310, 320, 330, and 340, see Figs. 8A and 8B) for executing a multiply instruction on a number (Data X and Data Y, see Figs. 7 and 8A) stored in the register pair (225, and 237, see Fig. 7), including first means (multiplier 311, see Fig. 8A) for performing multiply instructions on higher-order portions (Data X[0:1] and Data Y[0:1], see also Col. 12, lines 25-30) of each register in the register pair (225, and 237, see Fig. 7), second means (multiplier M in 320, see Figs. 8A and 8B) for performing multiply instructions on the remaining portions (Data X[2:3] and Data Y[2:3], see also Col. 12, lines 31-36) of each register in the register pair, and third means (Adder 353, see Fig. 8A, see also Col. 13, lines 6-7) for combining the results from the first and second means.

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Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 5,459,843).

Davis et al. discloses the claimed invention except for: the instruction fetch logic that fetches a single word into the two registers simultaneously (claim 3); and explicitly showing to use : an eight port general register file (claim 4) and the general register file including four read registers and four write registers (claim 5).

Davis et al. does disclose two registers (see Fig. 6, general purpose registers (A) 148, and general purpose register (B) 150, see also Col. 7, lines 16-18). However, it is well known in the art to fetch a single word into two registers simultaneously in order to speed up the fetch processing. Davis et al.'s registers (A) and (B) inherently comprise a plurality of read and write ports each. However, using an eight port general

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register file including four read registers and four write registers is an alternative arrangement as required in practice.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Davis et al.'s system to comprise the instruction fetch logic that fetches a single word into the two registers simultaneously, in order to increase the processor bandwidth and CPU performance for the Davis et al.'s system; and comprise an eight port general register file; and the general register file including four read registers and four write registers since they are just an alternative arrangement as required in practice comparing with that used in the Davis et al.'s system.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bloomgren et al. (US 5,781,750).

Referring to claim 6, Bloomgren et al. discloses, as claimed, a digital signal processor (see Fig. 2) capable of integrating subopcodes (RISC opcode, see Col. 5, lines 58-61, regarding the CISC instruction is broken down into several smaller RISC instructions) into an established instruction set (emulation code or emulation instruction set when in the emulation mode, see Col. 5, lines 48-49, and Col. 5, lines 58-61) comprising: a memory (IFETCH 32, see Fig. 2, and Col. 6, lines

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16-19) that stores instructions having opcodes (the opcodes see Tables 2-3); an instruction decoder (Emulation instruction Decoder (Emu ID) inside block 36, see Fig. 2) that identifies a relocatable opcode (CISC opcodes not directly supported by the hardware, see Col. 5, lines 53-55) to designate 64 subopcodes (RISC opcode, see Col. 5, lines 58-61, regarding the CISC instruction is broken down into several smaller RISC instructions); and a subopcode detector (RISC instruction Decoder (RISC ID) inside block 36, see Fig. 2) that decodes subopcodes if the instruction decoder (Emulation instruction Decoder (Emu ID) inside block 36, see Fig. 2) identifies the relocatable opcode (CISC opcodes not directly supported by the hardware, see Col. 5, lines 53-55).

Bloomgren et al. disclose the claimed invention except for comprising: 64 subopcodes: However, it is well known in the art that the number of the subopcodes is variable and changeable as required in practice.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Bloomgren et al.'s system to comprise 64 subopcodes since it is just an alternative arrangement as required in practice comparing with that used in the Bloomgren et al.'s system.

Allowable Subject Matter

10. The following is a statement of reasons for the indication of allowable subject matter: Davis et al., Gatherer et al., and Bloomgren et al., the closest references, do not teach or fairly suggest: a circular buffer control circuit comprising: means for restoring the address in the one of the circular buffer start registers associated with the selected circular buffer end register if the pointer matches the address in the selected circular buffer end register (claim 8).

11. Claims 9 and 10 are allowed.

12. The following is an examiner's statement of reasons for allowance: Davis et al., Gatherer et al., and Bloomgren et al., the closest references, and the other cited references, do not teach or fairly suggest:

a digital signal processor capable of executing zero overhead looping instruction commands comprising: second means for decrementing a loop count value stored in a second register within the register set; third means for executing another portion of the current instruction stored in a second portion of

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the first register and a second register within the register set (claim 9).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, such as Wilcox' 634; Dowling' 988; and Hendrie' 753 also disclose the similar limitations as claimed.

Contact Information

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to

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the TC 2100 receptionist whose telephone number is (703) 305-3900.

16. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number:

Official faxes: 703-746-7239; and

After Final faxes: 703-746-7238.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER

September 19, 2003